CLAIMS

1. A method of forming a transistor device, comprising:

providing a silicon-comprising surface;

exposing the silicon-comprising surface to activated nitrogen to form a peak nitrogen concentration within the silicon-comprising surface of at least 15% (atom percent);

providing a channel region on one side of the material comprising silicon and nitrogen;

providing a transistor gate structure on a side of the material comprising silicon and nitrogen that is opposed to said one side; and

forming a pair of source/drain regions separated from one another by the channel region.

2. The method of claim 1 further comprising forming a layer of silicon dioxide over the channel region, and wherein the silicon-comprising surface is a surface of the silicon dioxide.

3. The method of claim 1 wherein the transistor device is a PMOS device.

4. The method of claim 1 wherein the transistor device is an NMOS device.

5. The method of claim 1 further comprising subjecting the material comprising silicon and nitrogen to an anneal at a temperature of about 900°C for a time of from about 10 seconds to about 60 seconds; and wherein the material comprising silicon and nitrogen is heated to the anneal temperature by rapid thermal processing at a temperature ramp rate of at least about 10°C/second.

6. A method of forming a transistor device, comprising:

providing a silicon-comprising surface;

exposing the silicon-comprising surface to activated nitrogen for at least about 20 seconds to convert the silicon-comprising surface to a material comprising silicon and nitrogen; the activated nitrogen being formed by exposing a nitrogen-containing precursor to a plasma maintained at a power of at least about 750 watts;

providing a channel region on one side of the material comprising silicon and nitrogen;

providing a transistor gate structure on a side of the material comprising silicon and nitrogen that is opposed to said one side; and

forming a pair of source/drain regions separated from one another by the channel region.

7. The method of claim 6 further comprising forming a layer of silicon dioxide over the channel region, and wherein the silicon-comprising surface is a surface of the silicon dioxide.

8. The method of claim 6 wherein the transistor device is a PMOS device.

9. The method of claim 6 wherein the transistor device is an NMOS device.

10. The method of claim 6 wherein the plasma is maintained at a power of from about 1,500 watts to about 5,000 watts.

11. The method of claim 6 wherein the plasma is remote relative to the silicon-comprising surface.

12. The method of claim 6 wherein the plasma contacts the silicon-comprising surface.

13. The method of claim 6 further comprising maintaining the silicon-comprising surface at a temperature of from about 25°C to about 400°C during the exposing of the surface to the activated nitrogen.

14. The method of claim 6 further comprising subjecting the material comprising silicon and nitrogen to an anneal at a temperature of about 900°C for a time of from about 10 seconds to about 60 seconds.

15. The method of claim 6 further comprising subjecting the material comprising silicon and nitrogen to an anneal at a temperature of about 900°C for a time of from about 10 seconds to about 60 seconds; and wherein the material comprising silicon and nitrogen is heated to the anneal temperature by rapid thermal processing at a temperature ramp rate of at least about 10°C/second.

16. A method of forming a transistor device, comprising:

providing a semiconductor substrate having a silicon-comprising surface;

exposing the silicon-comprising surface to activated nitrogen for at least about 20 seconds to convert the silicon-comprising surface to a material comprising silicon and nitrogen; the activated nitrogen being formed by exposing a nitrogen-containing precursor to a plasma maintained at a power of at least about 750 watts;

forming a transistor gate structure over the material comprising silicon and nitrogen; the transistor gate structure being formed proximate a channel region; the material comprising silicon and nitrogen being between the transistor gate structure and the channel region; and

forming a pair of source/drain regions separated from one another by the channel region.

17. The method of claim 16 further comprising forming a layer of silicon dioxide over the channel region, and wherein the silicon-comprising surface is a surface of the silicon dioxide.

18. The method of claim 16 wherein the transistor device is a PMOS device.

19. The method of claim 16 wherein the transistor device is an NMOS device.

20. The method of claim 16 wherein the plasma is maintained at a power of from about 1,500 watts to about 5,000 watts.

21. The method of claim 16 wherein the plasma is remote relative to the silicon-comprising surface.

22. The method of claim 16 wherein the plasma contacts the silicon-comprising surface.

23. The method of claim 16 further comprising maintaining the silicon-comprising surface at a temperature of from about 25°C to about 400°C during the exposing of the surface to the activated nitrogen.

24. The method of claim 16 further comprising subjecting the material comprising silicon and nitrogen to an anneal at a temperature of about 900°C for a time of from about 10 seconds to about 60 seconds.

25. The method of claim 16 further comprising subjecting the material comprising silicon and nitrogen to an anneal at a temperature of about 900°C for a time of from about 10 seconds to about 60 seconds; and wherein the material comprising silicon and nitrogen is heated to the anneal temperature by rapid thermal processing at a temperature ramp rate of at least about 10°C/second.

26. A method of forming a transistor device, comprising:

providing a silicon-comprising material;

defining a channel region of the transistor device beneath the silicon-comprising material;

implanting a dopant into the channel region to a concentration of less than about 7×10^{17} atoms/cm^3 as a V_t implant;

forming a dielectric material over the channel region; the forming the dielectric material comprising exposing the silicon-comprising material to activated nitrogen to form a peak nitrogen concentration within the exposed dielectric material of at least about 15 atom percent;

forming a transistor gate structure over the nitrogen-comprising material; and

forming a pair of source/drain regions separated from one another by the channel region.

27. The method of claim 26 further comprising forming a layer of silicon dioxide over the channel region, and wherein the silicon-comprising material is the silicon dioxide.

28. The method of claim 26 wherein the transistor device is a PMOS device.

29. The method of claim 26 wherein the concentration of dopant in the V_t implant is less than 7×10^{17} atoms/cm^3.

30. The method of claim 26 wherein the concentration of dopant in the V_t implant is from about 1×10^{17} atoms/cm^3 to 7×10^{17} atoms/cm^3.

31. The method of claim 26 wherein the concentration of dopant in the V_t implant is from about 1×10^{17} atoms/cm^3 to 5×10^{17} atoms/cm^3.

32. The method of claim 26 wherein the activated nitrogen is formed from a plasma maintained at a power of from about 1,500 watts to about 5,000 watts.

33. The method of claim 26 wherein the activated nitrogen is formed from a plasma that is remote relative to the silicon-comprising material.

34. The method of claim 26 wherein the activated nitrogen is formed from a plasma that contacts the silicon-comprising material.

35. The method of claim 26 further comprising maintaining the silicon-comprising material at a temperature of from about 25°C to about 400°C during the exposing of the material to the activated nitrogen.

36. A method of forming a plurality of transistor devices, comprising:

providing a semiconductor substrate having a silicon-comprising surface;

defining a plurality of transistor device channel region locations beneath the silicon-comprising surface; the channel region locations being divided amongst a first group and a second group;

covering the silicon-comprising surface over the second group of transistor device channel region locations with a masking material;

while the masking material is over the second group of transistor device channel region locations, exposing the silicon-comprising surface over the first group of transistor device channel region locations to activated nitrogen for at least about 20 seconds to convert the silicon-comprising surface to a material comprising silicon and nitrogen; the activated nitrogen being formed by exposing a nitrogen-containing precursor to a plasma maintained at a power of at least about 750 watts;

removing the masking material;

after removing the masking material, forming transistor gate structures over the first and second groups of transistor device channel region locations; and

forming a plurality of source/drain regions; individual pairs of the source/drain regions being separated from one another by individual channel region locations.

37. The method of claim 36 further comprising forming a layer of silicon dioxide over the channel region locations, and wherein the silicon-comprising surface is a surface of the silicon dioxide.

38. The method of claim 36 wherein the transistor devices are all PMOS devices.

39. The method of claim 36 wherein at least some of the transistor devices are NMOS devices.

40. The method of claim 36 wherein the plasma is maintained at a power of from about 1,500 watts to about 5,000 watts.

41. The method of claim 36 wherein the plasma is remote relative to the silicon-comprising surface.

42. The method of claim 36 wherein the plasma contacts the silicon-comprising surface.

43. The method of claim 36 further comprising maintaining the silicon-comprising surface at a temperature of from about 25°C to about 400°C during the exposing of the surface to the activated nitrogen.

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